PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Andrew MORAN et al. — Group Art Unit: Unassigned

Application No.: Unassigned — Examiner: Unassigned

Filed: April 16, 2004 — Attorney Dkt. No.: 108347-00024 (089.0006)

For: MIXER CIRCUIT OFFSET COMPENSATION

CLAIM FOR PRIORITY

Director of the U.S. PTO
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The benefit of the filing date(s) of the following prior foreign application(s) in the following foreign country is hereby requested for the above-identified patent application and the priority provided in 35 U.S.C. §119 is hereby claimed:

British Patent Application No. 0309043.8 filed on April 22, 2003

In support of this claim, certified copy of said original foreign application is filed herewith.

It is requested that the file of this application be marked to indicate that the requirements of 35 U.S.C. §119 have been fulfilled and that the Patent and Trademark Office kindly acknowledge receipt of these/this document.

Please charge any fee deficiency or credit any overpayment with respect to this paper to Deposit Account No. 01-2300.

Respectfully submitted,

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Date: 4/16/04

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Dated 23 March 2004

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Statement of inventorship and of right to grant of a patent

The Patent Office

Cardiff Road
Newport
South Wales
NP9 1RH

1. Your reference — RL.P52426GB

2. Patent application number *(if you know it)* — 0309043.8

3. Full name of the or of each applicant

Zarlink Semiconductor Limited

4. Title of the invention

Mixer Circuit Offset Compensation

5. State how the applicant *(s)* derived the right from the inventor *(s)* to be granted a patent

By virtue of employment

6. How many, if any, additional Patents Forms 7/77 are attached to this form?
(see note (c))

7. I/We believe that the person *(s)* named over the page *(and on any extra copies of this form)* is/are the inventor *(s)* of the invention which the above patent application relates to.

Signature Marks & Clerk — Date 16 April 2003

8. Name and daytime telephone number of person to contact in the United Kingdom

Dr. Robert Lind
01865-397900

Notes

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d) When an application does not declare any priority, or declares priority from an earlier UK application, you must provide enough copies of this form so that the Patent Office can send one to each inventor who is not an applicant.

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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The Patent Office

1/77

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THE PATENT OFFICE
J
22 APR 2003
NEWPORT

The Patent Office

Cardiff Road
Newport
South Wales
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1. Your reference

RL.P52425GB

19APR03 E801418-2 001063
P01/7700 0.00-0309043.8

2. Patent application number
(The Patent Office will fill in this part)

0309043.8

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

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Patents ADP number *(if you know it)*

8177974001

If the applicant is a corporate body, give the country/state of its incorporation

United Kingdom

4. Title of the invention

Mixer Circuit Offset Compensation

5. Name of your agent *(if you have one)*

Marks & Clerk

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

4220 Nash Court
Oxford Business Park South
Oxford OX4 2RU
United Kingdom

7271125001

Patents ADP number *(if you know it)*

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

Patents Form 1/77

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	6
Claim *(s)*	2
Abstract	1
Drawing *(s)*	5

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	1
Request for preliminary examination and search *(Patents Form 9/77)*	1
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature Marks & Clerk Date 16 April 2003

12. Name and daytime telephone number of person to contact in the United Kingdom

Dr. Robert Lind
01865-397900

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MIXER CIRCUIT OFFSET COMPENSATION

The present invention relates to mixer circuit offset compensation and in particular, though not necessarily, to compensation for D.C. offsets in mixer circuits which give rise to local oscillator breakthrough.

Mixer circuits are commonly used to perform a frequency translation of a modulated input signal such that the output signal contains all the same phase and amplitude modulation present on the input signal translated onto a different output carrier frequency. The output carrier frequency can be either higher or lower than the frequency of the input carrier. These frequency translations are known respectively as upconversion and downconversion. Frequency translation of an input signal in this way necessarily results in degradation of the quality of the signal. Degradation is caused particularly by the addition of thermal noise, signal distortion through the use of non-linear components, the addition of signals harmonically related to both the frequency of the local oscillator used in the frequency translation and the input carrier frequency, leakage of the input signal to the output, and leakage of the local oscillator signal into both the input and the output. This latter effect is known as local oscillator "breakthrough".

Figure 1 shows a known balanced mixer circuit arrangement, known as a Gilbert cell mixer. The arrangement comprises generally an input stage 10, a mixer core 11, and a current source 12. The input stage comprises first and second npn transistors 13 and 14, each of which has its emitter electrodes connected to an output of the current source 12 by respective ones of emitter degeneration or series feedback resistors 15 and 16. The base electrodes of the first and second transistors 13,14 serve as the differential voltage inputs 13a,14a to the mixer circuit arrangement. The current source 12 includes a transistor 18, an emitter grounding resistor 19 and a capacitor 20, which is connected between the base electrode of the transistor 18 and ground potential. The base electrode of the transistor 18 is biased by a voltage source (not shown). The collector electrode of the transistor 18 forms the output of the current source 12. The current source 12 is a high impedance current source, which sets the quiescent current for the whole of the mixer circuit arrangement.

The mixer core 11 includes first to fourth npn transistors 21 to 24, the collector electrodes of which are cross-connected and connected to a supply line (V_{cc}) 25 by respective ones of load resistors 26 and 27. First and second output terminals 28 and 29 are connected to the lower terminals of the load resistors 26 and 27. Local oscillator input terminals 30 and 31 are connected to the base electrodes of the mixer core transistors 21 to 24.

Assuming that the Gilbert cell mixer is perfectly balanced, and in particular that the collector currents of the input stage transistors 13,14 are balanced, the output from the mixer core will consist mainly of the desired primary sidebands. However, any imbalance will tend to give rise to D.C. offsets in the circuit, one consequence of which will be local oscillator breakthrough into the output waveform of the mixer. Integrated Circuit (IC) layout techniques are optimised to achieve the best possible match, but this is limited by inherent mismatches found in IC devices, especially CMOS devices.

It is an object of the present invention to provide compensation for imbalance in a mixer circuit and thereby to reduce the effect of local oscillator breakthrough in the output.

According to a first aspect of the present invention there is provided a mixer circuit arrangement for frequency-translating a voltage input signal by an amount dependent on the frequency of a local oscillator signal to provide an output signal, comprising an input stage and a mixer stage, the input stage being arranged to convert the voltage input signal into differential current signals and the mixer stage being arranged to mix the differential current signals with the local oscillator signal to provide the output signal, characterised by means for injecting a compensation current into the input stage so as to balance the differential current signals provided to the mixer stage.

The means for injecting a compensation current into the input stage may comprise means for injecting the compensation current into a voltage input of the input stage, the voltage input being one of a pair of differential inputs for receiving said voltage input signal.

The means for injecting a compensation current into the input stage may comprise a memory for storing a predetermined compensation current value, and means for generating a compensation current corresponding to that value. For example, the value may be stored as a digital value, the means comprising a digital to analogue converter for converting the digital value into a corresponding analogue current. The means comprises a digitally controlled switch for selecting the voltage input of the input stage to which the compensation current is to be applied.

The means for injecting a compensation current into the input stage may comprise a resistor bridge coupling input voltages to the voltage inputs of the input stage, the compensation current being injected into the input stage via the resistor bridge.

Preferably, the mixer circuit arrangement including the means for injecting a compensation current into the input stage is integrated into a single chip.

According to a second aspect of the present invention there is provided a method of reducing local oscillator breakthrough in a mixer circuit arrangement for frequency-translating a voltage input signal by an amount dependent on the frequency of a local oscillator signal to provide an output signal, the mixer circuit comprising an input stage and a mixer stage, the input stage being arranged to convert the voltage input signal into differential current signals and the mixer stage being arranged to mix the differential current signals with the local oscillator signal to provide the output signal, the method comprising injecting a compensation current into the input stage so as to balance the differential current signals provided to the mixer stage.

For a better understanding of the present invention and in order to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 shows a prior art mixer circuit arrangement;

Figure 2 illustrates schematically a mixer circuit arrangement embodying the present invention;

Figure 3 shows a circuit detail of the mixer circuit arrangement of Figure 2 for generating a compensation current;

Figure 4A shows a circuit detail of the mixer circuit arrangement of Figure 2 for generating switching signals from a control input;
Figure 4B shows a circuit detail of the mixer circuit arrangement of Figure 2 for switching a compensation current between inputs of an input stage of the arrangement; and
Figure 5 shows a resistor network of the the circuit arrangement of Figure 2.

A prior art mixer circuit arrangement has already been described with reference to Figure 1. Figure 2 illustrates a modified balanced mixer arrangement in which a mixer core 32 corresponds to the mixer stage 11 of the arrangement of Figure 1. A voltage-current converter 33 corresponds to a combination of the input stage 10 and the current source 12 of the prior art arrangement. Circuit details are omitted from the circuit of Figure 2 for simplicity. It will be appreciated that this arrangement is given by way of example. Other features such as an interstage filter may be added to the arrangement.

Figure 2 shows a compensation current block 34 which is arranged to provide a compensation current to one of two outputs, I_{outp} and I_{outn}. These outputs are coupled to a resistor network 35, which has a pair of inputs coupled to the input voltage signal v_{inp} and v_{inn} and a pair of outputs coupled to voltage inputs of the voltage-current converter 33.

The compensation current block 34 comprises three main functional circuit components. A first of these components 35 is shown in Figure 3, and comprises a series of eight current mirrors 36 which are switched in and out in dependence upon the least 8 significant bits of a digital control word. (This control word is 9 bits in length – 8 bits for controlling the current mirrors and 1 bit for setting the polarity.) The component 35 receives at an input 37 a constant current reference signal I_{ref}, and provides at an output 38 an output current I_{out} which is a fractional value of the reference current. The digital control word is stored in a memory, not shown in the Figures.

Figure 4A shows a second functional circuit component 39 of the compensation current block 34. This receives at an input (V_{cntl}) 40 the most significant bit of the digital control word, and generates the complement of this bit at an output 41 (V_{cntlB}). The

third functional component 42 is illustrated in Figure 4B, and comprises a pair of current switches 43,44 which are switched on and off respectively by the control signals V_{cntl} and V_{cntlB}. The output current I_{out} provided by the circuit of Figure 3 is applied to a common current input 45 of the pair of switches. Depending upon the value of the most significant bit of the digital control word, the current I_{out} appears one or other of the outputs of the current switches, i.e. the second and third functional components together provide current steering towards either the positive or negative inputs of the resistor network 35.

Figure 5 illustrates in more detail the resistor network 35 of the circuit arrangement of Figure 2.

The operation of the embodiment described with reference to Figures 2 to 5 will now be explained. Following fabrication of the described mixer circuit, and with the digital control word programmed to be zero, the differential output voltage of the mixer stage is analysed for a range of input signals and for one or more local oscillator frequencies. Using an appropriate algorithm, the value of the digital control word which would minimise the local oscillator breakthrough could be determined. This control word aims to provide an offset current into the input stage which is equal to but of opposite polarity to the D.C. offset which is giving rise to the local oscillator breakthrough. The memory is programmed with this word, and tests run to determine whether or not this value produces optimum results. If not, the value may be tweaked, i.e. adjusted up or down.

Rather than using some algorithm to determine a suitable value for the digital control word, the digital control word may be determined empirically. A typical value may be programmed to the memory, and the results analysed. Depending upon the direction and magnitude of the change in local oscillator breakthrough, the value is adjusted up or down. This process is repeated until the optimum value is determined.

It will be appreciated that the resolution of the offset compensation mechanism is dependent upon the size of the digital control word and the number of current mirrors in the circuit of Figure 3.

Although a Gilbert cell mixer arrangement has been described hereinbefore, other arrangements, for example using any other type of transconductor, could be used. Such transconductors include micro mixer circuits, single balanced mixers and the like, including transconductors having differential inputs, as long as a differential current signal is provided as an output signal.

It will be appreciated by the person of skill in the art that various modifications may be made to the above described embodiments without departing from the scope of the present invention.

CLAIMS:

1. A mixer circuit arrangement for frequency-translating a voltage input signal by an amount dependent on the frequency of a local oscillator signal to provide an output signal, comprising an input stage and a mixer stage, the input stage being arranged to convert the voltage input signal into differential current signals and the mixer stage being arranged to mix the differential current signals with the local oscillator signal to provide the output signal, characterised by means for injecting a compensation current into the input stage so as to balance the differential current signals provided to the mixer stage.

2. A circuit according to claim 1, the means for injecting a compensation current into the input stage comprising means for injecting the compensation current into a voltage input of the input stage, the voltage input being one of a pair of differential inputs for receiving said voltage input signal.

3. A circuit according to claim 1 or 2, the means for injecting a compensation current into the input stage comprising a memory for storing a predetermined compensation current value, and means for generating a compensation current corresponding to that value.

4. A circuit according to claim 3, the value being stored as a digital value, and the means comprising a digital to analogue converter for converting the digital value into a corresponding analogue current.

5. A circuit according to claim 4, said means comprising a digitally controlled switch for selecting the voltage input of the input stage to which the compensation current is to be applied.

6. A circuit according to any one of the preceding claims, the means for injecting a compensation current into the input stage comprising a resistor bridge coupling input voltages to the voltage inputs of the input stage, the compensation current being injected into the input stage via the resistor bridge.

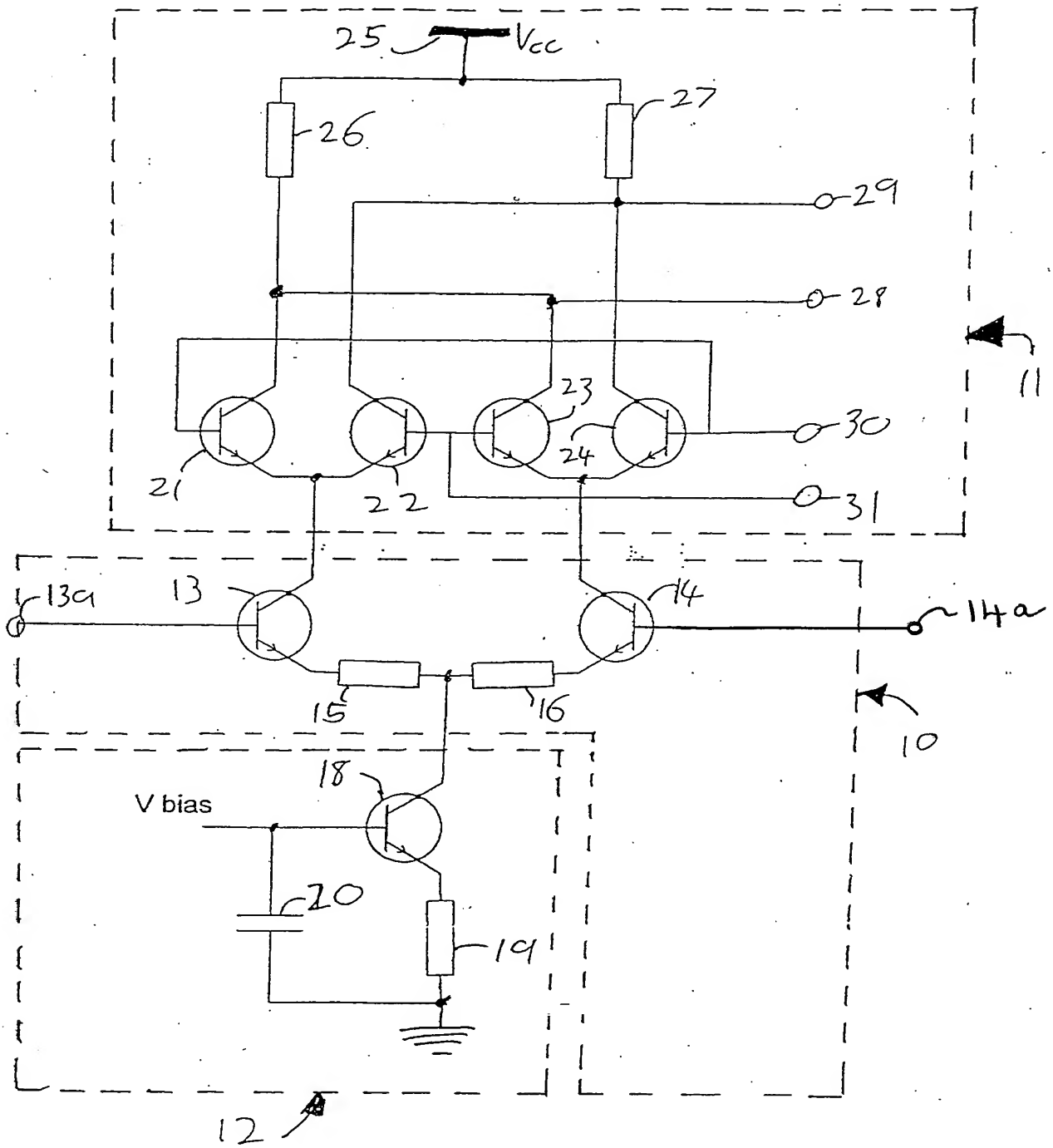
7. A method of reducing local oscillator breakthrough in a mixer circuit arrangement for frequency-translating a voltage input signal by an amount dependent on the frequency of a local oscillator signal to provide an output signal, the mixer circuit comprising an input stage and a mixer stage, the input stage being arranged to convert the voltage input signal into differential current signals and the mixer stage being arranged to mix the differential current signals with the local oscillator signal to provide the output signal, the method comprising injecting a compensation current into the input stage so as to balance the differential current signals provided to the mixer stage.

ABSTRACT

MIXER CIRCUIT OFFSET COMPENSATION

A mixer circuit arrangement for frequency-translating a voltage input signal by an amount dependent on the frequency of a local oscillator signal to provide an output signal. The arrangement comprises an input stage 33 and a mixer stage 32, the input stage 33 being arranged to convert the voltage input signal into differential current signals and the mixer stage 32 being arranged to mix the differential current signals with the local oscillator signal to provide the output signal. Means 34,35 is provided for injecting a compensation current into the input stage 33 so as to balance the differential current signals provided to the mixer stage 32.

(Figure 2)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28
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23
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13a
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14a
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V bias
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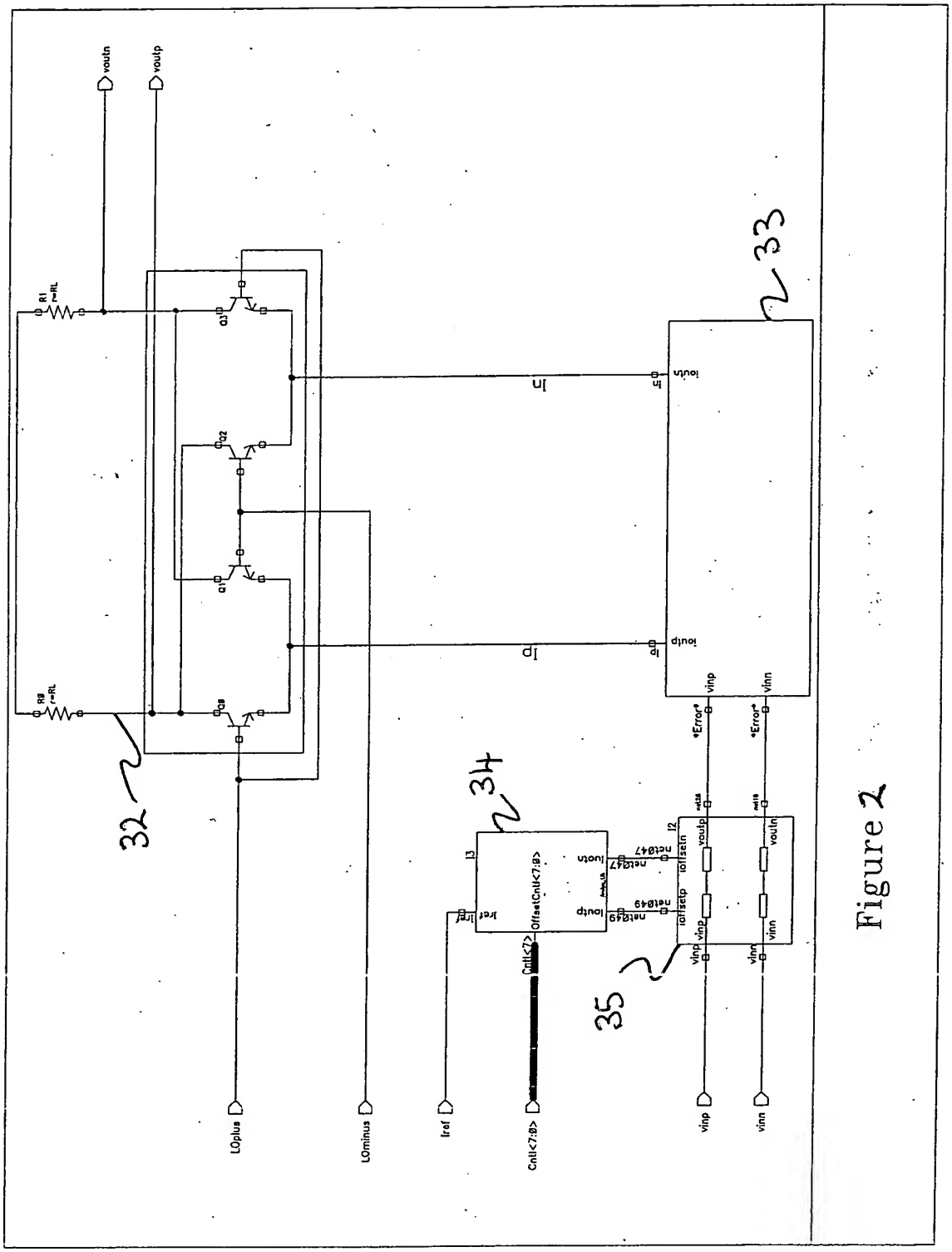
19
12

FIGURE 1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voutp
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RL
R0
RL
Q0
Q1
Q2
Q3
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33
34
35
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ioutp
vinp
vinn
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voutn
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ioffsetn
net049
net047
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I1
I2
I3
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LOminus
Iref
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vinp
vinn

Figure 2

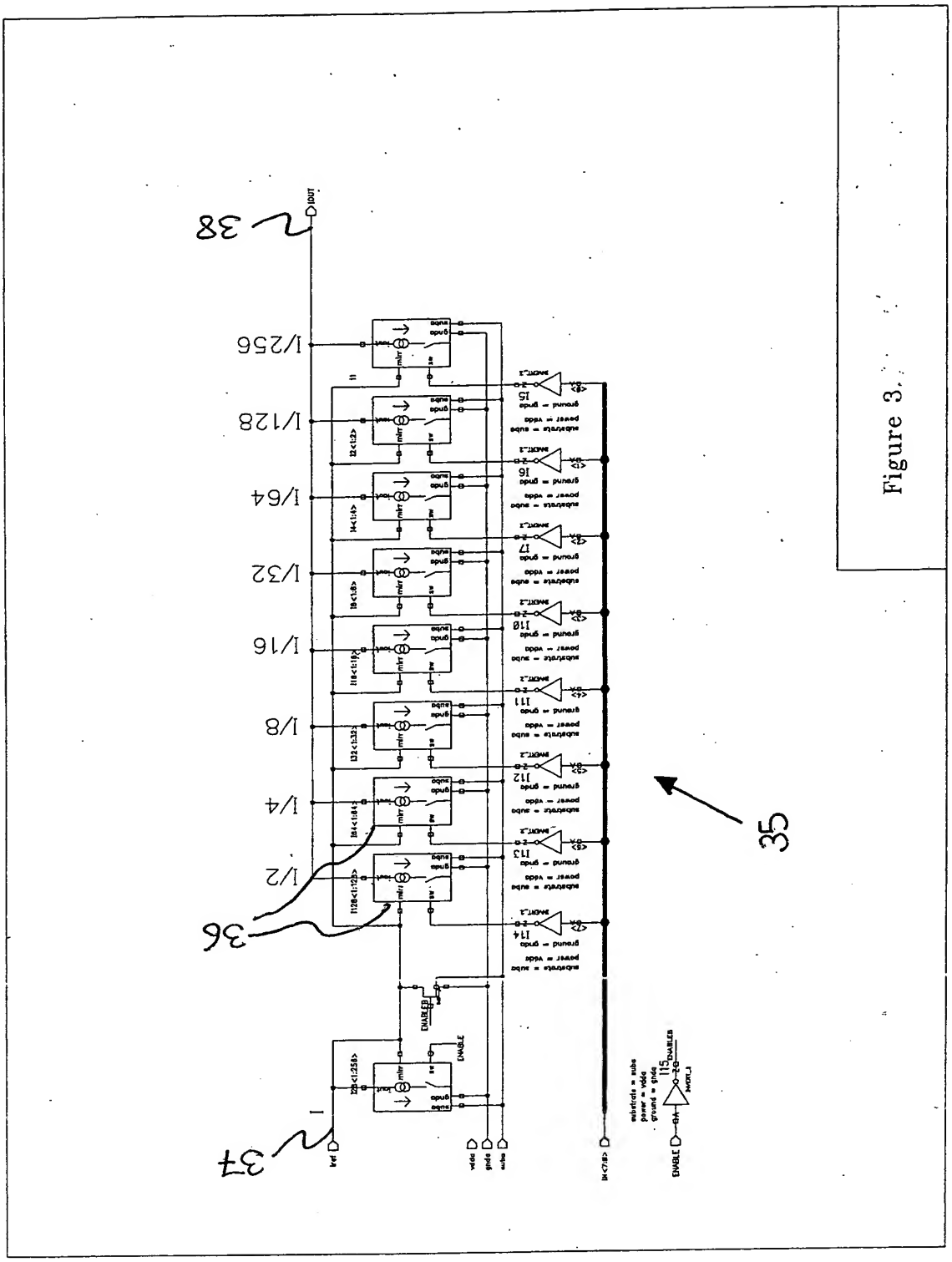
38
37
36
35
I/256
I/128
I/64
I/32
I/16
I/8
I/4
I/2
IOUT
Iref
ENABLE
ENABLEB
substrate = subs
power = vdda
ground = gnda
ENABLE
ENABLEB

Figure 3.

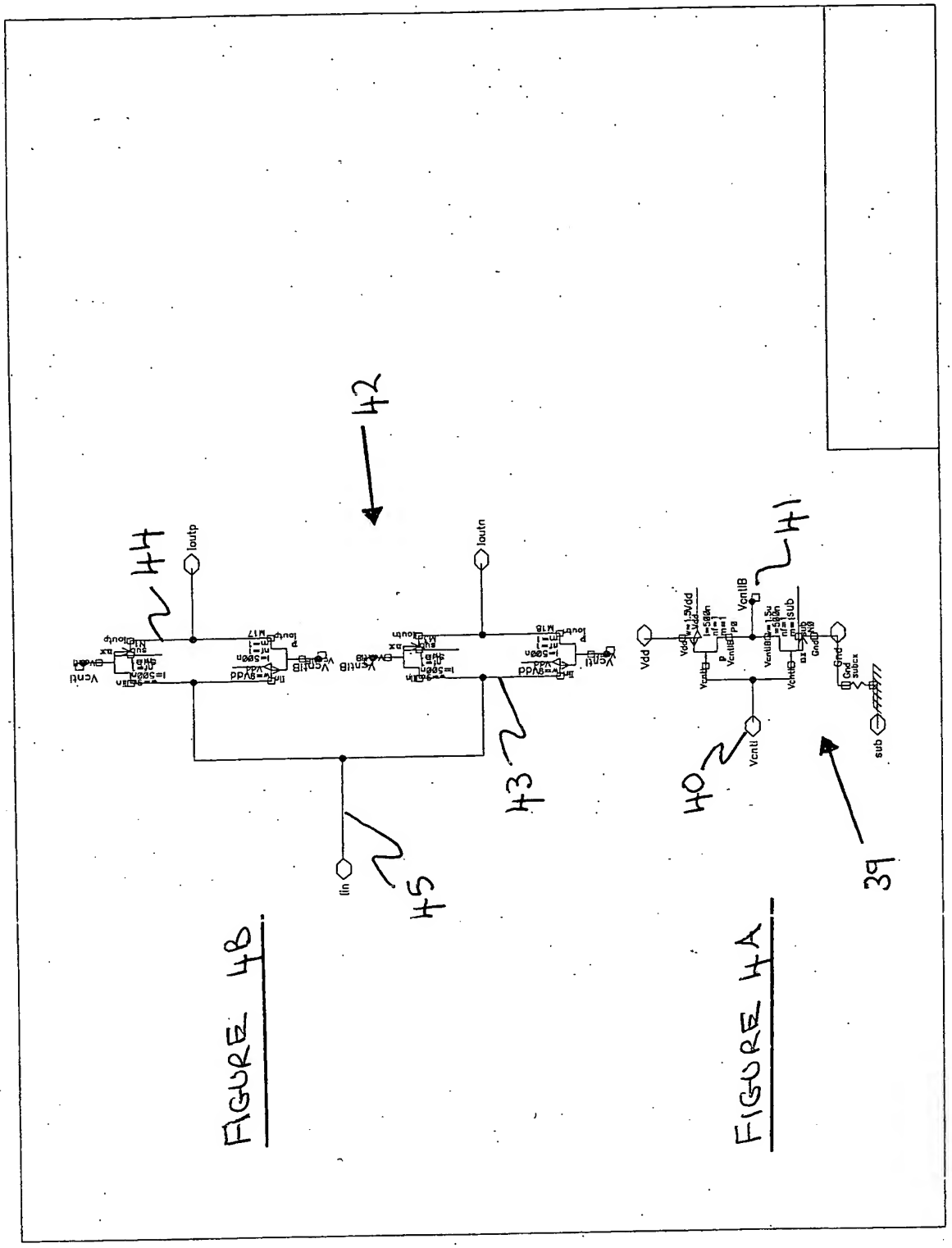

FIGURE 4B

FIGURE 4A

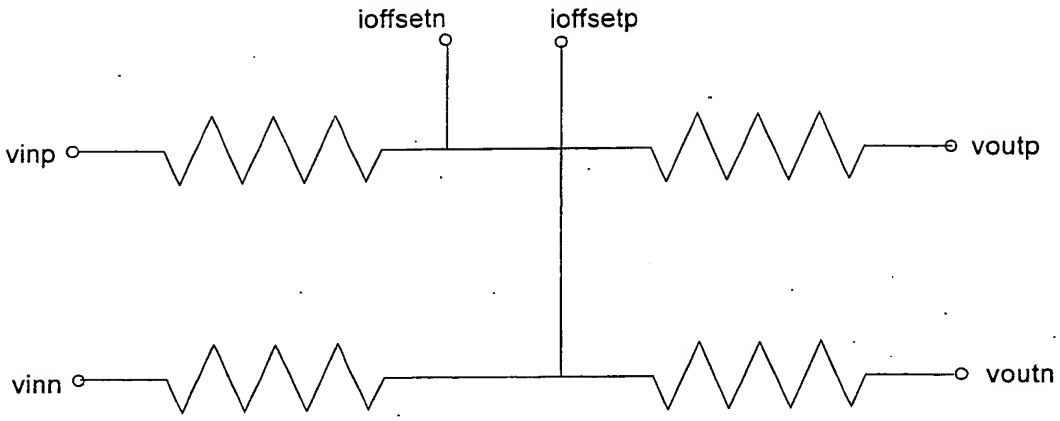

Figure 5

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Docket No.: 108347-0024
Serial No: Unassigned - Filed: April 16, 2004
Inventors): Andrew MORAN et al.